Amendments to the Drawings:

Please insert "prior art" to the caption of Figure 2e. The Appendix contains a replacement drawing sheet.

REMARKS/ARGUMENTS

Claims 1-7 are pending in the application; reexamination and reconsideration are hereby requested.

Claims 1-5 were rejected as unpatentable over Wang; the Examiner pointed to Wang generally for MAP decoding and asserted cascade architecture is known in MAP decoding.

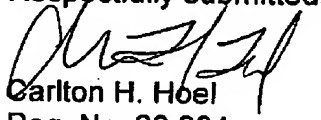
Applicants reply that claim 1 requires the forward and backward recursion blocks to each have a cascade architecture. In contrast, Wang appears to use parallel processing (see column 2, lines 44-50; column 8, lines 6-15). Wang has no suggestion of cascade architecture. Further, table A (Wang column 10) counts computations, not numbers of ACS units as required by claim 4.

Claims 6-7 were rejected as unpatentable over Yagyu in view of Wang; the Examiner pointed to Yagyu for iterative turbo decoding and used Wang as before.

Applicants repeat their foregoing argument that Wang (plus Yagyu) does not suggest the cascade architecture for the recursion blocks.

Claims 1, 4, and 6 have been amended as suggested by the Examiner.

Respectfully submitted,



Carlton H. Hoel
Reg. No. 29,934
Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, Texas 75265
972.917.4365